

**United** International **University** (UIU)

Dept. of Electrical and Electronic Engineering (EEE)

# **Course**: VLSI Design Lab (EEE 442)

**Experiment 4: Physical Design of a Counter**

Introduction:

1. Switch to csh, this will also setup your cadence tools environment variables

* csh

1. Create the lab directory and few other sub-directories under your work area:

* mkdir lab4
* cd lab4
* mkdir lib constraints lef physical\_design netlist

1. Copy the gate level netlist from previous lab into the netlist/ sub-directory

* cp ../lab3/synthesis/cntr8bit\_netlist.v netlist/

1. Copy the SDC constraint from previous lab into the constraints/ sub-directory

* cp ../lab3/synthesis/cntr8bit.sdc constraints /

1. Copy the .lib files from previous lab into the lib/ sub-directory

* cp ../lab3/lib/\*.lib lib/

1. Copy the LEF (Library Exchange Format) file from ~sahmed/eee442/lab4/lef/

* cp ~sahmed/eee442/lab4/lef/all.lef lef/

1. Go to physical\_design/ and invoke Innovus Tool to do the Place & Route the design. This will launch the Innovus Tool in the GUI mode.

* cd physical\_design
* innovus

DESIGN IMPORT

1. Click on *File 🡪 Import Design* menu option. This will open the *Design Import* window.
2. Under *Netlist:* option choose *Verilog*. Click on the browse button to select the gate level netlist from the netlist/ sub-directory
3. Under *Top Cell:* option select *Auto Assign:*
4. Under *Technology/Physical Libraries:* option select *LEF Files:* Click on the browse button and select all.lef file from lef/ sub-directory
5. Under *Power* option use **VDD** as *power Nets:* **VSS** as *Ground Nets:*
6. Under *analysis Configuration* option click on the *Create Analysis Configuration* button.
7. An *MMMC Browser* window will open.
8. Double click on *Library Sets*. *Add Library Set* window will open. *Name:* it as **max\_timing** and click on ‘Add…’ button under ‘Timing Library Files’
9. Set **max\_timing** to ‘slow.lib’ and **min\_timing** to ‘fast.lib’ under the lib/ sub-directory.
10. Double click on *Delay Corners*. *Add Delay Corner* window will appear. *Name:* it as **min\_delay**. In the ‘Library Set’ option under ‘Attributes’, scroll to **min\_timing** and click ‘OK’
11. Similarly set **max\_delay** to **max\_timing**.
12. Double click on *Constraints Modes*. *Add Constraint Mode* window will open. *Name:* it as **counter\_constraints** and click on ‘Add…’ button under ‘CDS Constraint Files’
13. Set **counter\_constraints** to ‘cntr8bit.sdc’ under constraints/ sub-directory.
14. Double click on *Analysis Views*. *Add Analysis View* window will open. *Name:* it as **worst\_case** and select **max\_delay** for *Delay Corner* and click ‘OK’
15. Similarly set **best\_case** to **min\_delay**.
16. Double click on *Setup Analysis Views*. *Add Setup Analysis Views* window will open. Set the *Analysis View* to **worst\_case**. Click ‘OK’
17. Double click on *Hold Analysis Views*. *Add Hold Analysis Views* window will open. Set the *Analysis View* to **best\_case**. Click ‘OK’
18. *MMMC Browser* will look as below: Click on ‘Save & Close’.
19. *Save MMMC View Definition File* window will open. Provide the *File name:* as **Default.view** and click on ‘Save’
20. Click ‘OK’ on the *Design Import* window. This will load the design into Innovus

FLOOR PLANNING

1. Click *Floorplan 🡪 Specify Floorplan* menu option. This will open the ‘Specify Floorplan’ window.
2. Select aspect ratio as per requirement. Give some dimension in ‘Core to Left’, ‘Core to Right’, ‘Core to Top’ and ‘Core to Bottom’. (Remember the values are in µm) to create space for Power Rings. After defining code are, click ‘OK’

POWER PLANNING

1. Click on *Power 🡪 Power Planning 🡪 Add Rings* menu option. This will open ‘Add Rings’ window
2. Type/Select **VDD** and **VSS** nets under the *Net(s)* option.
3. Select top/bottom layers as Metal5, left/right layers as Metal6. Make sure the metal layer names match with that of all.lef file in lef/ sub-directory. Set the width/space as per requirement (unit is in µm) and taking the space between core boundary and I/O pad consideration. Select the option for offset as ‘Center in channel’ and click ‘OK’
4. Power ring will be created between core boundary and IO/Die boundary
5. Click *Power 🡪 Power Planning 🡪 Add Stripe* menu option. This will open ‘Add Stripes’ window
6. Type/Select **VDD** and **VSS** nets under the *Net(s)* option.
7. Select *Layer:* as Metal6 and *Direction:* as *Vertical*. Make sure the metal layer names and direction match with that of all.lef. Set width/spacing as per requirement (unit is in µm). Choose one of the *Set* Pattern, use *Core ring* as the *Stripe Boundary*, set the *First/Last Stripe* staring from *left*. Click ‘OK’.
8. Vertical power stripe will be created.
9. Perform steps 34, 35 and 36 to create horizontal stripes if needed.
10. Click *Route 🡪 Special Route* menu option. This will open ‘SRoute’ window
11. Type/Select **VDD** and **VSS** nets under the *Net(s)* option.
12. Choose any of the options I*Follow Pins* for standard cells) that you want to ruote under *SRoute*
13. Choose the *Top/Bottom Layer* and other option as needed. Click ‘OK’
14. This will create the standard cell rails and others if chosen

PLACEMENT

1. Click *Place 🡪 Place Standard Cells* menu option. This will open ‘Place’ window
2. Select ‘Run Full Placement’, choose ‘Include Pre-Place Optimization’ under *Optimization Option*. Click ‘OK’
3. Click on the *Physical View* to see the standard cells.

PRE-CTS TIMING

1. Click *Timing 🡪 Report Timing* menu option. This will open ‘Timing Analysis’ window
2. Select ‘Pre-CTS’ under *Design Stage* and ‘Setup’ under *Analysis Type*. Click ‘OK’
3. This will display the timing information on the Innovus terminal. Carefully check the Worst Negative Slack (WNS) and Total Negative Slack (TNS).
4. If there are WNS/TNS, click on *Optimize 🡪 Optimize Design* menu option. This will open ‘Optimization’ window
5. Select ‘Pre-CTS’ under *Design Stage* and ‘Setup’, ‘Max Cap’ and ‘Max Tran’ under *Optimization Type*. Click ‘Ok’. This will optimize the design. Check timing again. Repeat until timing is met.

CLOCK TREE SYNTHESIS

1. Click *Clock 🡪 Synthesize Clock Tree…’* menu option. This will open ‘Synthesize Clock Spec’ window
2. Click on ‘Gen Spec…’ This will open ‘Generate Clock Spec’ window
3. From *Cells List* select all cells starting with ‘CLK’ and click on ‘Add’ button to add them to the *Selected Cells*. Give a name for the *Output Specification File:* and click ‘OK’.
4. Give a name for the *Result Directory:* in the ‘Synthesis Clock Tree’ window. Click ‘OK’

ROUTING

1. …
2. …

VERIFICATION

1. Geometry
2. Connectivity
3. …

GDS Out

1. …